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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,234	07/09/2003	Shigeki Tomishima	009683-469	8323

7590 04/03/2006

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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,234	TOMISHIMA ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This final Office action is in response to the amendment filed 27 February 2006. Claims 1-4 are pending. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Dreibelbis et al. [U.S. 5,875,470], hereinafter "Dreibelbis".

As to claim 1, Dreibelbis teaches a memory device (Figure 1A; Figure 1B; Figure 2) comprising:

a memory unit (Bank 1.1-4.4 in Figure 1A); and

an arbiter (combination of Bank Address Control 10 in Figure 1A, Crosspoint Switch 20 in Figure 1B, and I/O Selection Control 21 in Figure 1B) controlling said memory unit while arbitrating (Address 16, Figure 1A; 5-1 to 5-4, Figure 1A; column 6, lines 20-24; Column 6, Lines 55-62; Column 6, Lines 25-31; Column 5, Lines 1-5; Column 8, Lines 28-31; Column 7, Lines 23-31) for bus access requests (Column 5, lines 57-60; Column 6, lines 15-24; Column 2, lines 57-67) from a plurality of units outside the memory unit (Processors 1-4, Figure 3; Column 6, lines 15-16), wherein

when a second bus access request takes place before an access to said memory unit that corresponds to a first bus access request has been completed, said arbiter performs activation of said memory unit that corresponds to said second bus access request in parallel with writing or reading data to/from said memory unit that corresponds to said first bus access request (Column 5, Lines 2-5; Column 5, Lines 61-63; Column 6, Lines 25-31; the prior art also recites, in numerous places, that Dreibelbis' memory device allows simultaneous accesses by multiple processors to multiple memory banks, see Column 4, Lines 64-67; Column 5, Lines 1-5. If there are simultaneous accesses to the memory banks, then the memory unit must be activated by the arbiter in response to the second request before the first access has been completed. It is also clear an memory access is either a writing or reading to/from the memory unit) after an address signal is input to said memory unit (it is clear an address signal has already been input to the memory unit for the first access in order for it to be carried out, see Column 5, Lines 1-5, Column 5, Lines 60-64; Column 6, Lines 15-24).

As to claim 3, Dreibelbis discloses a plurality of memory banks (Column 2, lines 6-9; Column 4, lines 57-60; Banks 1.1-4.4, Figure 1A; Figure 2) in the disclosed memory device. The arbiter of the memory device has a plurality of address ports (Items 10, 11-1 to 14-4, Figure 1A) corresponding to the said plurality of units (Column 2, lines 17-20; Column 4, line 64 to Column 5 line 5; Column 5, lines 27-36; Column 6, lines 15-20). Furthermore, the arbiter outputs an address for the second bus access request in parallel with the first access to a first bank (Column 5, lines 61-65; Column 6, lines 15-24; output second address in parallel with the first access if the bank accessed by the second address is not busy), in order to activate a second memory bank (Column 5, lines 2-5).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dreibelbis [U.S. 5,875,470], in further view of Fadavi-Ardekani et al. [US 6,401,176 B1] (hereinafter "Fadavi-Ardekani").

As for claim 2, Dreibelbis already substantially discloses the claim as described above, and further teaches that said arbiter outputs a rejection signal that corresponds to a second bus access request before the access to said memory unit that corresponds to said first bus access request has been completed (see Column 5, lines 39-44), but fails to teach that the signal is an acknowledge signal. However, Fadavi-Ardekani teaches a memory arbitration system (see Abstract) wherein an acknowledge signal is sent to in order to indicate the granting of the shared resource to the winning requestor (see Column 4, lines 23-57). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combined Fadavi-Ardekani's teaching with that of Dreibelbis' so that Dreibelbis' "arbiter outputs an acknowledge signal that corresponds to said second bus access request ... " in order to indicate the granting of the shared resource to the requesting unit.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dreibelbis [U.S. 5,875,470], further in view of Masuoka et al. [U.S. 6,472,714].

As for claim 4, Dreibelbis substantially discloses the memory device as described above, but does not teach a memory device that contains the units that make the bus access requests. However, it is obvious to one ordinarily skilled in the art at the time of the applicant's invention that a single chip embedded system such as System-on-Chip (SoC) has the advantages of higher performance, less power consumption, better reliability, and lower cost. Therefore, Dreibelbis' memory device would benefit from these advantages by making it a single chip device containing the units that make the bus access requests. Furthermore, Masuoka et al. teaches a SoC device that comprises memory and a plurality of units including a CPU for controlling the operation of the memory, and the increased degree of integration of the SoC device resulted in reduced area and improved operating speed (Column 1, lines 8-22). It would have been obvious to one ordinarily skilled in the art at the time of the applicant's invention that Dreibelbis' memory device would have improved operating speed and reduced area if it contained the plurality of units.

Response to Arguments

7. Applicant's arguments have been considered, but the newly added limitations are taught by Dreibelbis as set forth above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

28 March 2006

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER